

REMARKS

Applicant thanks the Examiner for acknowledging receipt of Applicants' foreign priority document that has been submitted pursuant to 35 USC section 119. Applicant has also made the drawing modifications requested by the Examiner in the office action.

Applicant respectfully requests reconsideration of the prior art rejections set forth by the Examiner under 35 USC sections 102 and 103. Applicant respectfully submits that the prior art references of record, whether considered alone or in combination fail to either teach or suggest Applicant's presently claimed invention.

More specifically, Applicant's claimed invention is directed to an improved imaging device having a charge transfer structure wherein the last group of transfer electrodes has three regions each with distinct potential levels located directly beneath the electrodes. In contrast, the prior art Hirota reference cited by the Examiner merely discloses a transfer device wherein the transfer electrodes are two phase driven and there are only two distinct regions beneath each of the transfer electrodes including the last pair of transfer electrodes. In Hirota, to the extent that a third region with a different potential exists, the region is not located beneath the transfer electrodes.

A review of the cited art confirms that neither Hirota nor any of the other remaining references of record provide the requisite teaching or suggestion of Applicant's claimed structure. Accordingly, in light of the foregoing, Applicant requests that the Examiner now withdraw the rejections and allow all claims in the application.

Appl. No. 09/621,651
Amdt. Dated February 9, 2004
Reply to Office Action of October 7, 2003

Respectfully submitted

Date: February 9, 2004

(Reg. #37,607)

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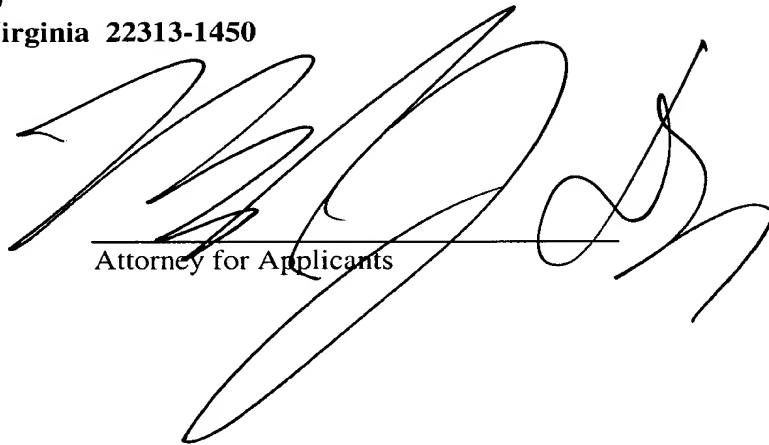
Attorney for Applicant

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CERTIFICATE OF MAILING

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P.O. Box 1450
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Attorney for Applicants



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PRIOR ART

FIG. 5A

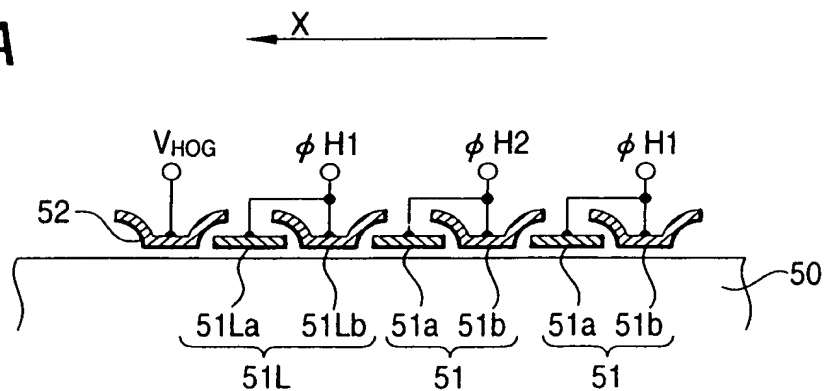


FIG. 5B

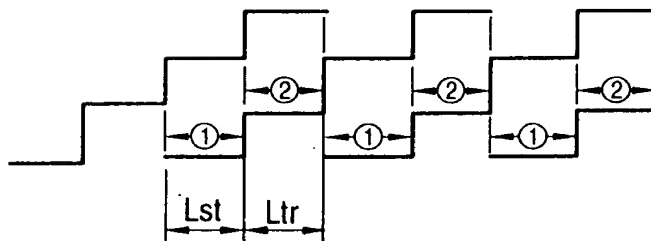
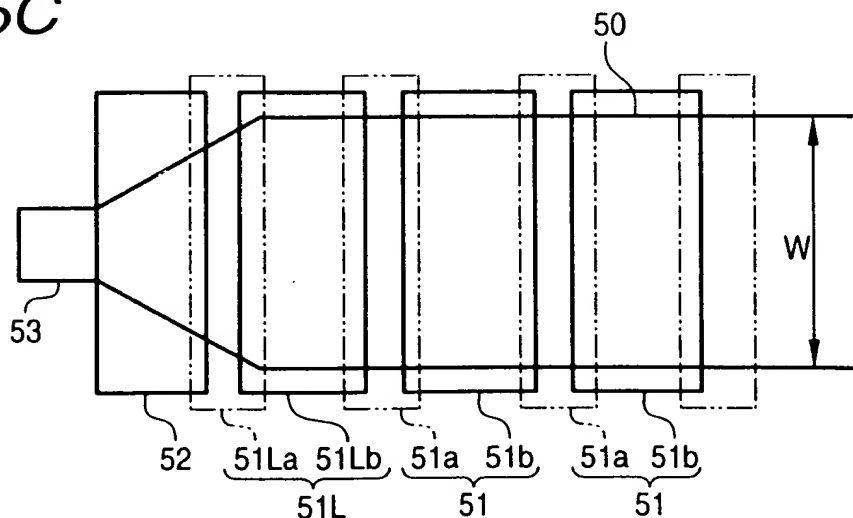


FIG. 5C





PRIOR ART^{6/7}

FIG. 6A

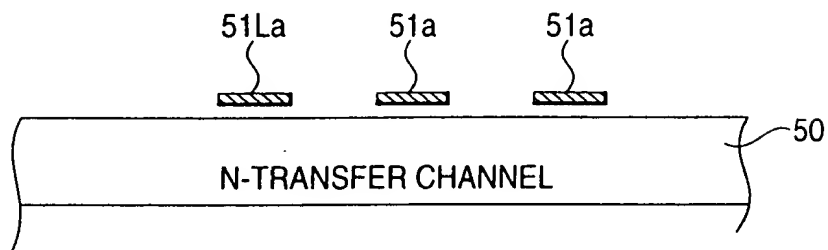


FIG. 6B

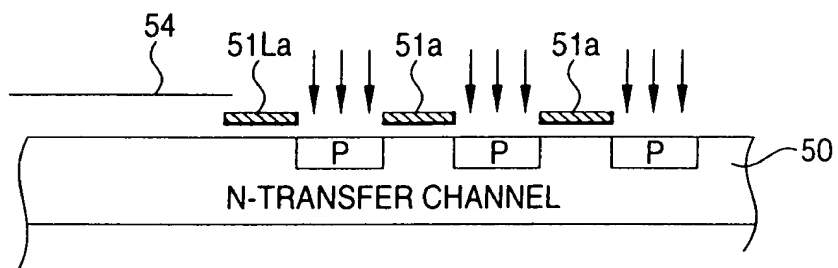


FIG. 6C

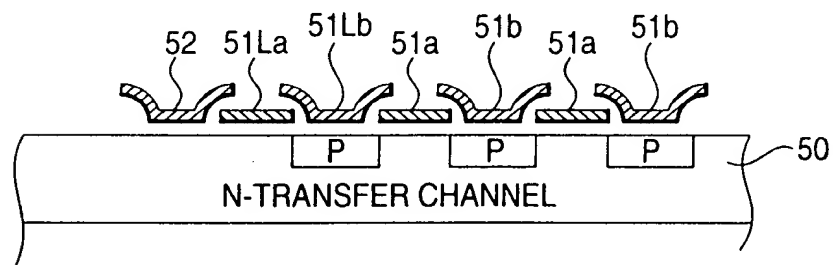
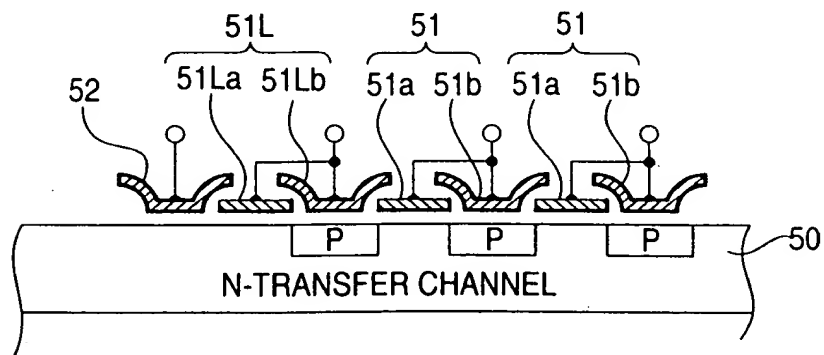
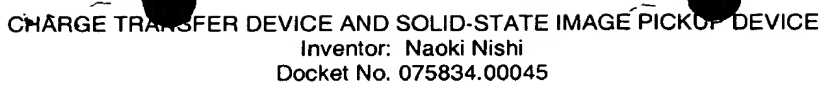


FIG. 6D





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PRIOR ART

A cross-sectional view of a semiconductor device. It shows a substrate 50 with a series of gates 51. The gates are divided into regions 51La, 51Lb, 51a, and 51b. A layer 52 is on top of the gates. A layer 53 is on the left. Dimensions Lst and Ltr are indicated. Electrical connections are shown at the bottom, labeled V_{HOG} , $\phi H1$, $\phi H2$, and $\phi H1$.